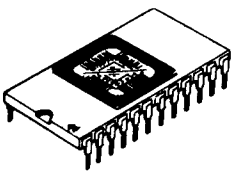
HN462716, HN462716G

2048-word×8-bit UV Erasable and Electrically Programmable Only Memory

The HN462716 is a 2048 word by 8 bit erasable and electrically programmable ROMs. This device is packaged in a 24-pin, dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

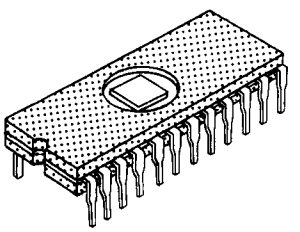
- Single Power Supply ..... +5V ±5%
- Simple Programming .....Program Voltage: +25V DC
  Programs with One 50ms Pulse
- Static ..... No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Fully Decoded-on Chip Address Decode
- Access Time ..... 450ns Max.
- Low Power Dissipation .....555mW Max. Active Power
  213mW Max. Standby Power
- Three State Output ..... OR- Tie Capability
- Interchangeable with Intel 2716

HN462716



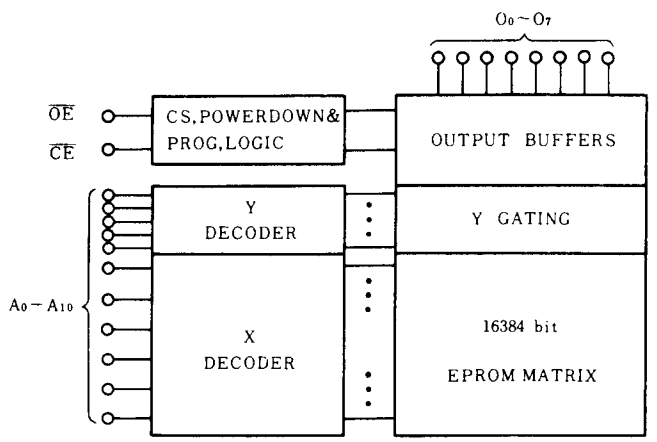
(DC-24C)

HN462716G

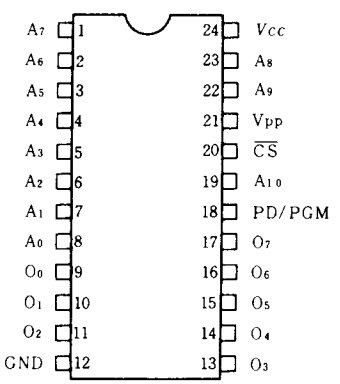


(DG-24B)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ PROGRAMMING OPERATION

Mode \ Pins	$\overline{CE}$ (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	Outputs (9~11, 13~17)
Read	V_{IL}	V_{IL}	+5	+5	Dout
Deselect	Don't Care	V_{IH}	+5	+5	High Z
Power Down	V_{IL}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	Din
Program Verify	V_{IL}	V_{IL}	+25	+5	Dout
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	℃
Storage Temperature Range	T_{stg}	−65 to +125	℃
All Input and Output Voltages*	V_{IN}, V_{OUT}	−0.3 to +7	V
V_{PP} Supply Voltage*	V_{PP}	−0.3 to +28	V

* with respect to Ground

■ READ OPERATION

• DC AND OPERATING CHARACTERISTICS (Ta=0 to +70℃, V_{CC}=5V± 5%, V_{PP}=V_{CC}±0.6V)

Item	Symbol	Test Condition	min.	typ.	max.	Unit.
Input Leakege Curreut	I_{LI}	V_{IN}=5.25V	—	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=5.25V/0.4V	—	—	10	μA
V_{PP} Current	I_{PP1}	V_{PP}=5.85V	—	—	5	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$=V_{IH}, $\overline{OE}$=V_{IL}	—	21	35	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{OE}$=$\overline{CE}$=V_{IL}	—	62	100	mA
Input LowVoltage	V_{IL}		−0.1	—	0.8	V
Input High Voltage	V_{IH}		2.0	—	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−400μA	2.4	—	—	V

Note: Vcc must be applied simultaneously or before Vpp and removed simultaneously or after Vpp.

• AC CHARACTERISTICS (Ta=0 to +70℃, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address to Output Delay	t_{ACC}	$\overline{OE}$=$\overline{CE}$=V_{IL}	—	—	450	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$=V_{IL}	—	—	450	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$=V_{IL}	—	—	120	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$=V_{IL}	0	—	100	ns
Address to Output Hold	t_{OH}	$\overline{OE}$=$\overline{CE}$=V_{IL}	0	—	—	ns

• CAPACITANCE (Ta=25℃, f=1MHz)

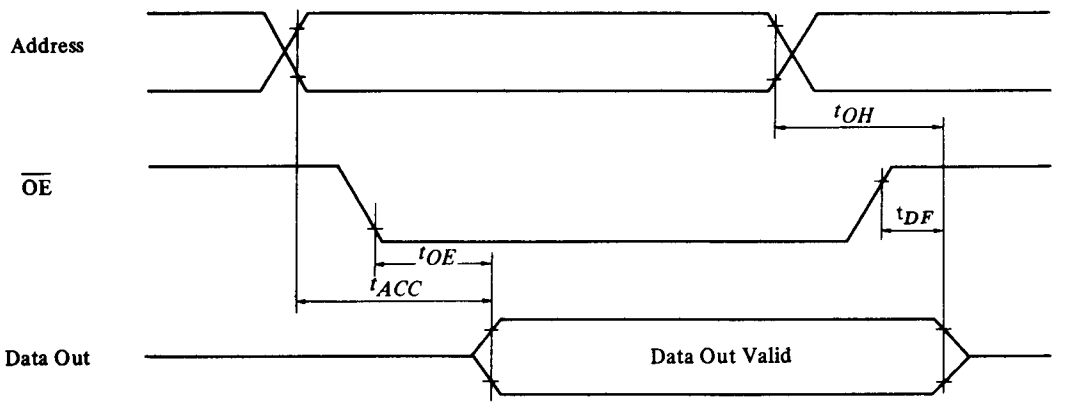
Item	Symbol	Test Condition	typ.	max.	Unit
Input Capacitance	C_{in}	V_{IN}=0V	—	6	pF
Output Capacitance	C_{out}	V_{OUT}=0V	—	12	pF

• SWITCHING CHARACTERISTICS

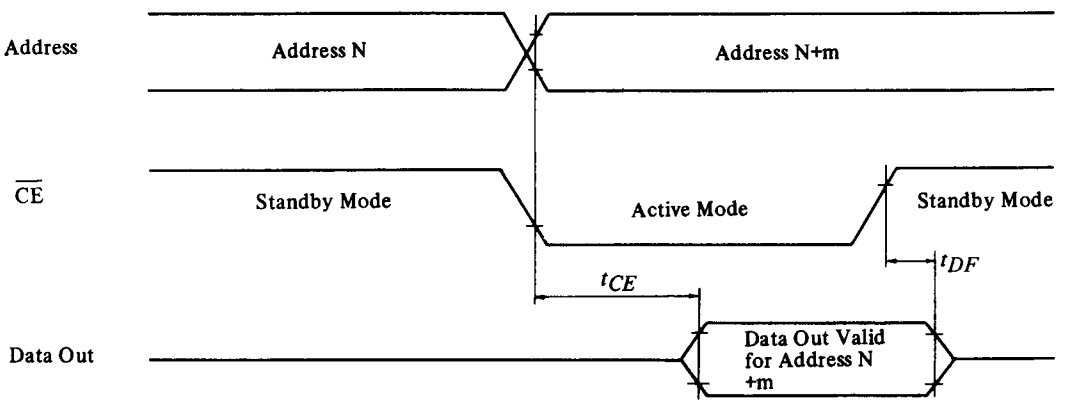
Test Conditions

Input Pulse Levels: 0.8V to 2.2V
Input Rise and Fall Times: ≤ 20 ns
Output Load: 1TTL Gate + 100 pF
Reference Level for Measuring Timing:
Inputs 1V and 2V
Outputs 0.8V and 2V

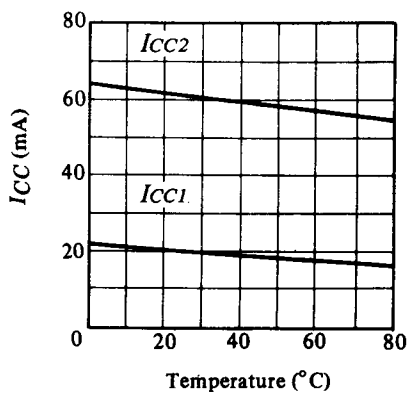
READ MODE ($\overline{CE}$ = V_{IL})

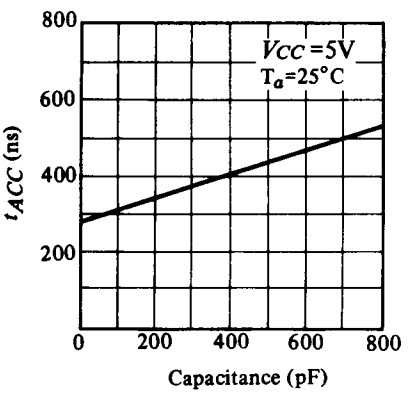


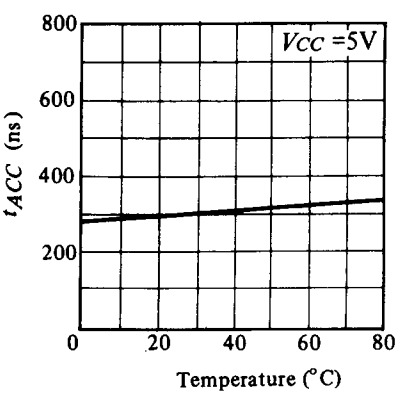
STANDBY MODE ($\overline{OE}$ = V_{IL})



• TYPICAL CHARACTERISTICS







• D.C. PROGRAMMING CHARACTERISTICS (Ta=25℃ ±5℃, V_{CC}=5V±5%, V_{PP}=25V±1V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{CC}=5.25V/0.4V	—	—	10	μA
V_{PP} Supply Current	I_{PP1}	$\overline{CE}=V_{IL}$	—	—	6	mA
V_{PP} Supply Current During Programming	I_{PP2}	$\overline{CE}=V_{IH}$	—	—	30	mA
V_{CC} Supply Current	I_{CC}		—	—	100	mA
Input Low Level	V_{IL}		−0.1	—	0.8	V
Input High Level	V_{IH}		2.0	—	V_{CC}+1	V

• A.C. PROGRAMMING CHARACTERISTICS (Ta=25℃ ±5℃, V_{CC}=5V±5%, V_{PP}=25V±1V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		2	—	—	μs
$\overline{OE}$ Hold Time	t_{OEH}		5	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay	t_{DF}	$\overline{CE}=V_{IL}$	0	—	120	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}=V_{IL}$	—	—	120	ns
Program Pulse Width	t_{PW}		45	50	55	ms
Program Pulse Rise Time	t_{PRT}		5	—	—	ns
Program Pulse Fall Time	t_{PFT}		5	—	—	ns

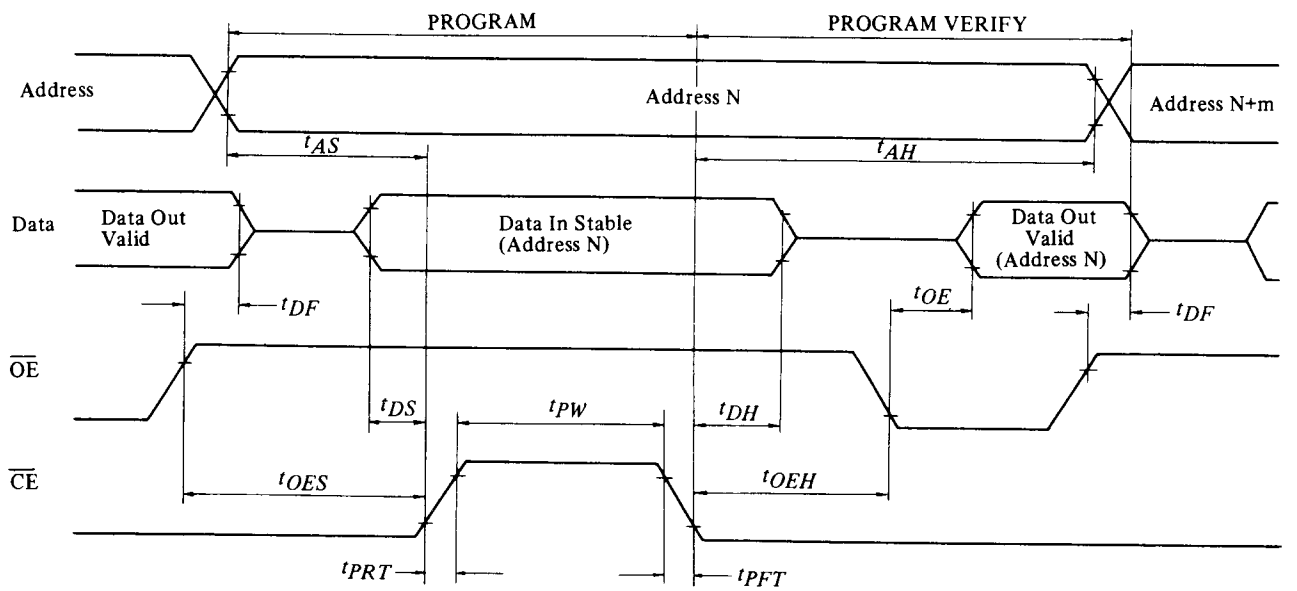
Note: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

• SWITCHING CHARACTERISTICS

Test Conditions
Input Pulse Level: 0.8V to 2.2V
Input Rise and Fall Times: ≤ 20 ns

Output Load: 1 TTL Gate + 100 pF
Reference Level for Measuring Timing:
Inputs; 1V and 2V, Outputs; 0.8V and 2V

• PROGRAMMING WAVEFORMS



• ERASE

Erasure of HN462716 is performed by exposure to ultraviolet light with a wavelength of 2537Å, and all the output data are changed to "1" after this erasure procedure.

The minimum integrated close (i.e., UV intensity x exposure time) for erasure is 15W · sec/cm^2.

■ DEVICE OPERATION

• READ MODE

Dataout is available 450 ns (t_{ACC}) from addresses with $\overline{OE}$ low or 120 ns (t_{OE}) from $\overline{OE}$ with addresses stable.

• DESELECT MODE

The outputs may be OR-tied together with the other HN462716s. When HN462716s are deselected, the $\overline{OE}$ inputs must be at high TTL level.

• POWER DOWN MODE

Power down is achieved with $\overline{CE}$ high TTL level. In this mode the outputs are in a high impedance state.

• PROGRAMMING

Initially, and after each erasure, all bits of the HN462716 are in the "high" state (Output High). Data is introduced by selectively programming "low" into the desired bit locations. In the programming mode, Vpp power supply is at 25V and $\overline{OE}$ input is at high TTL level. Data to be programmed are presented 8-bits in parallel, to the data output lines (O1 to O8).

The addresses and inputs are at TTL levels.

After the address and data setup, a 50 ms, active high program pulse is applied to the $\overline{CE}$ input. The $\overline{CE}$ is at TTL level.

The HN462716 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

• PROGRAM VERIFY

The HN462716 has a program verify mode. A verify should be performed on the programmed bits to determine that they were correctly programmed. In this mode Vpp is at 25V.

• PROGRAM INHIBIT

Programming of multiple HN462716s in parallel with different data is easily accomplished by using this mode. Except for $\overline{CE}$, all like inputs of the parallel HN462716s may be common.

A TTL program pulse applied to 0 HN462716's $\overline{CE}$ input will program that HN462716. A low level $\overline{CE}$ inhibits the other HN462716s from being programmed.